Listing of Claims

1. (Currently Amended) A system for correcting duty-cycle distortion, comprising:

a measurement circuit ~~unit~~ to measure duty-cycle distortion in a first clock signal, the measurement circuit including:

(a) a single-input charge pump driven by the first clock signal,

(b) a loop filter to output a voltage corresponding to an average of current from the charge pump over a predetermined time, and

(c) a bias generator to generate an analog correction signal based on the voltage output from the loop filter; and

a correction circuit ~~unit~~ to dynamically adjust a delay of at least one edge of a second [[the]] clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal being generated based on the second clock signal.

2. (Currently Amended) The system of claim 1, wherein the delay adjustment by the correction ~~unit~~ circuit causes ~~adjusts~~ durations of high-phase and low-phase portions of the second clock signal be adjusted to reduce the duty-cycle distortion in the first clock signal to substantially zero.

3-5 (Canceled)

6. (Currently Amended) The system of claim 1 [[5]], wherein the analog correction ~~control~~ signal adjusts ~~the duty cycle of~~ the at least one edge of the second clock signal by an amount which corrects substantially all the duty-cycle distortion in the first clock signal.

7. (Canceled)

8. (Currently Amended) The system of claim 1 [[5]], wherein the single-input charge pump ~~measurement unit~~ includes:

a signal generator ~~which generates the analog control signal, said signal generator including a control unit;~~

first and second switches;

a positive current source; and

a negative current source,

wherein the first and second switches to respectively connect ~~control unit selectively connects~~ the positive current source and the negative current source to an output node ~~of the signal generator~~ to generate the charge pump current to be averaged ~~analog control signal~~.

9. (Currently Amended) The system of claim 8, wherein the first and second switches to connect ~~control unit connects~~ the positive current source and the negative current source to the output node for different periods of time based on the duty cycle of the first clock signal to generate the charge pump current to be averaged ~~analog control signal~~.

10. (Currently Amended) A duty-cycle correction circuit, comprising:

a detection circuit to receive a first clock signal having duty-cycle distortion; and

a voltage-controlled buffer to continuously adjust a delay of at least one edge of a second ~~generate an output clock signal based on an input~~ clock signal [[and a]] to reduce the duty-cycle distortion in the first clock signal, the first clock signal generated based on the second clock signal and the buffer to delay the at least one edge of the second clock signal

based on an analog control voltage [[;]] received from the detection circuit, the detection circuit including:

(a) a single-input charge pump to receive the first ~~a core~~ clock signal and a bias voltage; and

(b) a bias generator to generate the bias voltage and said analog control voltage input into the buffer based on an average current output from [[of]] the single-input charge pump ~~and to feedback said control voltage to the single input charge pump~~.

11. (Currently Amended) The circuit of claim 10, wherein the voltage-controlled buffer corrects the second ~~input~~ clock signal to produce ~~have~~ reduced phase distortion in the first clock signal.

12. (Currently Amended) The circuit of claim 10, further comprising:

a startup circuit to generate an initial DC bias voltage for the single-input CP; and

a loop filter to ~~provide~~ generate a correction voltage corresponding to the average charge pump current, [[to]] the bias generator to generate the analog control voltage based on the correction voltage generated by the loop filter.

13. (Canceled)

14. (Original) The circuit of claim 10, wherein the bias generator compensates for changes in a supply voltage.

15. (Currently Amended) The circuit of claim 11, wherein a response time of the system to reduce said phase distortion is approximately 50 nS.

16. (Currently Amended) The circuit of claim 10, wherein the first ~~further comprising: a global clock network to distribute the output~~ clock signal is received from a global clock network.

17-18 (Canceled)

19. (Currently Amended) A method for correcting duty-cycle distortion, comprising:

measuring duty-cycle distortion in a first clock signal by:

(a) driving a single-input charge pump with the first clock signal,

(b) generating a voltage corresponding to an average of current output from the charge pump over a predetermined time, and

(c) generating an analog correction signal based on the voltage output from the loop filter; and

dynamically adjusting [[the]] a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal generated based on the second clock signal.

20. (Currently Amended) The method of claim 19, wherein a loop filter generates the average charge pump current ~~measuring the duty-cycle distortion includes: measuring~~ based on durations of high-phase and low-phase portions of the first clock signal.

21. (Currently Amended) The method of claim 20, ~~further comprising: generating an analog control signal based on said durations,~~ wherein the delay of the at least one edge of the second clock signal is adjusted based on the analog correction signal to cause the duration of the high-phase portion of the first clock signal to at least substantially equal the duration of the low-phase portion of the first clock signal.

22. (Currently Amended) The method of claim 19 [[21]], wherein the analog correction ~~control~~ signal adjusts ~~the duty cycle of~~ the at least one edge of the second clock ~~frequency~~ signal by an amount which corrects substantially all the duty-cycle distortion in the first clock signal.

23. (Canceled)

24. (Currently Amended) A processing system, comprising:

a circuit; and

a correction circuit [[unit]] to correct duty-cycle distortion of a first frequency signal input into the circuit, said correction unit comprising:

a measurement unit to measure duty-cycle distortion in the first frequency ~~a clock~~ signal, the measurement circuit including:

(a) a single-input charge pump driven by the first frequency signal,

(b) a loop filter to output a voltage corresponding to an average of current from the charge pump over a predetermined time, and

(c) a bias generator to generate an analog correction signal based on the voltage output from the loop filter; and

a correction unit to dynamically adjust a delay of at least one edge of a second frequency ~~the clock~~ signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first frequency signal, the first frequency signal generated based on the second frequency signal.

25. (Original) The processing system of claim 24, wherein said circuit includes a chipset, processor, or memory.

26. (New) The system of claim 1, wherein the correction circuit to adjust a delay of a first edge of the second clock signal based on the analog correction signal from the bias generator and maintains a second edge of the second clock signal at a fixed delay, to reduce the duty-cycle distortion in the first clock signal.

27. (New) The circuit of claim 1, wherein the buffer to adjust a delay of a first edge of the second clock signal based on the analog control voltage from the bias generator and maintains a second edge of the second clock signal at a fixed delay, to reduce the duty-cycle distortion in the first clock signal.

28. (New) The method of claim 19, wherein dynamically adjusting includes:

adjusting the delay of the first edge of the second clock signal based on the analog correction signal; and

maintaining a second edge of the second clock signal at a fixed delay to reduce the duty-cycle distortion in the first clock signal.

29. (New) The system of claim 24, wherein the correction unit to adjust a delay of a first edge of the second frequency signal based on the analog correction signal from the bias generator and maintains a second edge of the second frequency signal at a fixed delay, to the duty-cycle distortion in the first frequency signal.

30. (New) The system of claim 1, wherein the analog correction signal is indicative of an offset voltage generated by the charge pump current as a result of the duty-cycle distortion in the first clock signal.

31. (New) The system of claim 1, wherein the analog correction signal is inversely proportional to the voltage that corresponds to the average current from the charge pump over said predetermined time.

32. (New) The system of claim 1, wherein the correction circuit includes a voltage-controlled buffer comprising:

a buffer circuit;

a cascode amplifier coupled to the buffer circuit, the buffer circuit to delay the at least one edge of the second clock signal by an amount controlled a bias voltage generated by the cascode amplifier based on the analog correction signal from the bias generator.

33. (New) The system of claim 31, wherein the buffer circuit includes:

at least one inverter to invert the second clock signal; and

a plurality of current sources to set a drive strength of the at least one inverter based on the bias voltage from the cascode amplifier.

34. (New) The system of claim 33, wherein the current sources set the drive strength by controlling a transition slope of a signal output from the inverter, to thereby adjust high-phase and low-phase portions of the first clock signal

35. (New) The system of claim 34, wherein the bias voltage is inversely proportional to the analog correction signal.

36. (New) The system of claim 31, wherein the cascode amplifier includes:

an active load;

a first transistor coupled to the active load;

a second transistor connected to the first transistor; and

a current-source transistor coupled to the second transistor and having a gate coupled to receive the analog correction signal, the active load to output the bias voltage for controlling the buffer circuit.

37. (New) The system of claim 36, wherein the active load includes a diode-connected transistor.

38. (New) The system of claim 37, wherein the diode-connected transistor outputs the bias voltage in inverse proportion to the analog correction signal.

39. (New) The system of claim 38, wherein the first and second transistors and the current-source transistor are of a first conductivity and the diode-connected transistor is of a second opposing conductivity.

40. (New) The system of claim 38, wherein the first and second transistors and the current-source transistor are maintained in a same state.